JITTER ESTIMATION FOR A PHASE LOCKED LOOP

Abstract

A method for estimating jitter in a phase locked loop is provided. The estimation is determined from a simulation that uses a representative power supply waveform having noise as an input. Further, a computer system for estimating jitter in a phase locked loop is provided. Further, a computer-readable medium having recorded thereon instructions adapted to estimate jitter in a phase locked loop is provided.

23884_1.DOC